APPLICATION GUIDE

TRIP RELAY AND OPTO INPUT IMMUNITY ISSUES

Location: L:\UK Sales\5 APPLICATIONS\2 SECTION REPORTS\Application Guides\Trip Relay & Opto Input Immunity Issue.doc

SUMMARY

This document details the immunity issues faced by DC tripping and auxiliary relays together with optically isolated (opto) inputs on modern numerical relays. Particular attention is paid to AC induced voltage from surrounding current carrying conductors and the affects of capacitance discharge caused by station battery earth faults.

The aim of this document will provide sufficient guidance to ensure that such issues are correctly dealt with at the project planning stage rather than at a later date which can be costly to correct.

Title	Name	Signature	Date
Senior Applications Engineer	A Wixon BEng (Hons) CEng MIET		09/02/2012

T&D
Automation & Information Systems - St Leonards Avenue – Stafford – ST17 4LX – England
Tel: +44 (0)1785 223251 – Fax: +44 (0)1785 212232

Table of Contents

1. INTRODUCTION

This document outlines the application issues associated with tripping and auxiliary relays together with opto isololated inputs in numerical relays. Devices such as these will be susceptible to electrical environment aspects such as battery earth faults and induced AC quantities from adjacent current carrying conductors.

Whilst standards exist outlining the application of such devices, mistakes are commonly made leading to unexpected and costly mal-operations. The purpose of this document is to clarify the main application difficulties commonly encountered and offers workable solutions to each issue.

2. HIGH AND LOW BURDEN DEVICES

The burden of a protective device defines the power required for operation. Devices with a high input impedance will draw a lower current and hence require a lower power for operation. These devices would be considered as low burden. High burden devices, on the other hand, have a much lower input impedance leading to a higher operating current requirement.

The burden of the device has a direct impact on the relays stability during battery earth faults and induced ac signals. It can be proven that high burden devices are inherently more stable than their low burden counterparts, at the expense of increased battery drain. Clearly a balance must be struck between immunity and the limitation of battery drain, particularly for continuously operated devices.

This section discusses the types of devices that may be used together with their designated application.

2.1. TRIPPING AND AUXILIARY RELAYS

2.1.1. Auxiliary Relays (Type MVAA & PRIMA)

These relays are primarily designed for contact logic and contact multiplication purposes and are generally a low burden design (typically <3W) due to the fact that they are often continuously energised. In many cases these contacts are reserved for circuit breaker status, event recording and alarm annunciation purposes. However, circuit breaker tripping and closing is not recommended with such relays due to their poor immunity and relatively slow operating time (typically 12 to 25ms). Both of these issues are characteristics of the low burden design.

2.1.2. Tripping Relays (Type MVAJ)

These relays are designed for tripping of circuit breakers by virtue of their high speed (≤10ms) and immunity which are characteristics of a high burden design. In addition to tripping, these relays are also used for closing of the circuit breaker. Whilst speed is less important for closing of the circuit breaker the immunity of the relay is equally important to that of tripping applications. There are two main types of tripping relay, which are designed to conform to ESI standards these are :-

Relay Type	Standard	Minimum Operating Current	Typical Burden	Capacitive Immunity
Low Burden	ESI 48-4 EB1	≥10mA (30 & 48V models) ≥25mA (110/125V models)	25 Watts	Not Specified
High burden	ESI 48-4 EB2	≥20mA (30 & 48V models) ≥50mA (110/125V models)	150 Watts	10µF at 150V

In general, low burden relays are for applications where the trip wiring remains in the same room (i.e. short distances). High burden relays, on the other hand, are designed for applications where the trip relay is remote from the protective relay or where the trip wiring leaves the confines of the relay room. Naturally there are exceptions to these rules which are discussed in detail later.

2.1.3. Interposing Relays (Type MVAW)

Interposing relays are designed for environments where high levels of ac induced voltage are likely. This is typical for "cross site" intertripping and closing in high voltage substations, where even high burden tripping relays would not be suitable. Unlike tripping relays which obtain there immunity from their burden, interposing relays achieve there immunity by other means, such as a shunt capacitor and / or a "tubular copper slug". The capacitor allows some of the induced ac signal to bypass the operating coil thus providing a moderate level of immunity. The copper slug, which sleeves the core of the hinged armature unit, creates an opposing flux for ac signals therefore reducing the operating flux to practically zero. The ac immunity comes at the expense of operating speed which is typically 50 to 80ms.

2.2. OPTICALLY ISOLATED (OPTO) INPUTS

Opto inputs, such as those found in the MiCOM range, are commonly used for CB status recognition, trip circuit supervision and protection signalling. Examples of protection signalling would include buchholz alarm and trip, together with intertrip send and receive commands. Their low burden design makes them susceptible to AC interference and the capacitance discharge caused by battery earth faults. Some opto input circuits have additional filters (e.g. MiCOM Px40), which provide total immunity to AC signals and partial immunity to capacitance discharge. Further immunity to the capacitance discharge issues can be provided by the inclusion of a shunt resistor across the opto circuit. The parallel resistor also reduces the steady state voltage across the opto during battery earth faults, which is useful particularly for opto inputs with no settable threshold.

More advanced opto inputs are available in the AGILE range of protection relays. In addition to AC immunity filters, AGILE optos also have a dynamic impedance which makes them immune to capacitance discharge, without the need for parallel resistors. This method involves lowering the opto impedance for a fraction of a second, in order to discharge the capacitance before the opto can mal-operate.

This document discusses the general selection criteria of the shunt resistor, however, the precise value and wattage will vary with relay type and model.

3. AFFECTS OF BATTERY EARTH FAULTS

Much like any electrical circuit, substation battery wiring may experience faults from time to time. While short circuits are invariably cleared by the fuses, an earth fault may remain un-cleared due the circuit earth impedance. This leaves the circuit in a faulted state, which may lead to the following :-

- An impulse discharge through the relay coil / opto due to wiring capacitance
- A steady state voltage across the relay coil / opto
- A steady state "trickle" current through the relay coil / opto

The above factors will depend upon the position of the fault (positive or negative rail), the length of the DC wiring, the type of earthing and the type / presence of battery monitoring equipment.

The following section discusses the different types of fault and the affects they have on the connected devices, such as tripping / auxiliary relays and opto inputs.

NOTE: Substation batteries are normally supplied unearthed. The battery alarm may effectively be used to "high impedance" earth the DC supplies. This gives greater security as the integrity of the DC auxiliary supply will not be compromised by a single earth fault.

3.1. CENTRE TAPPED BATTERY – STEADY STATE CURRENT / VOLTAGE

This is the most common type of battery earthing currently in use. In many cases the earthing is provided by the battery monitoring device such as Alstom's BA300. Such devices limit the earth fault current to a relatively low magnitude and also limit the voltage across the device to typically less than 50% (assuming R1=R2) of the nominal battery voltage (V_{DC}). When calculating the maximum current and voltage that the device is subject to, it is prudent to assume that the battery is on boost charge at 125% of nominal (i.e. 1.25 V_{DC}).

Stability of the protective device is paramount during a battery earth fault. To establish the steady state stability of the protective device, the current and voltage must be determined. The following sections illustrate how the steady state current and voltage is calculated for each of the devices discussed earlier.

3.1.1. Tripping / Auxiliary Relays – steady state current

Since these devices are effectively Ampere-Turn driven, it essential that the steady state "trickle" current (I_{SS}) does not exceed the relay operating threshold. Figure 3.1 illustrates the steady state current path during the battery earth fault and also shows the calculation for I_{SS}.

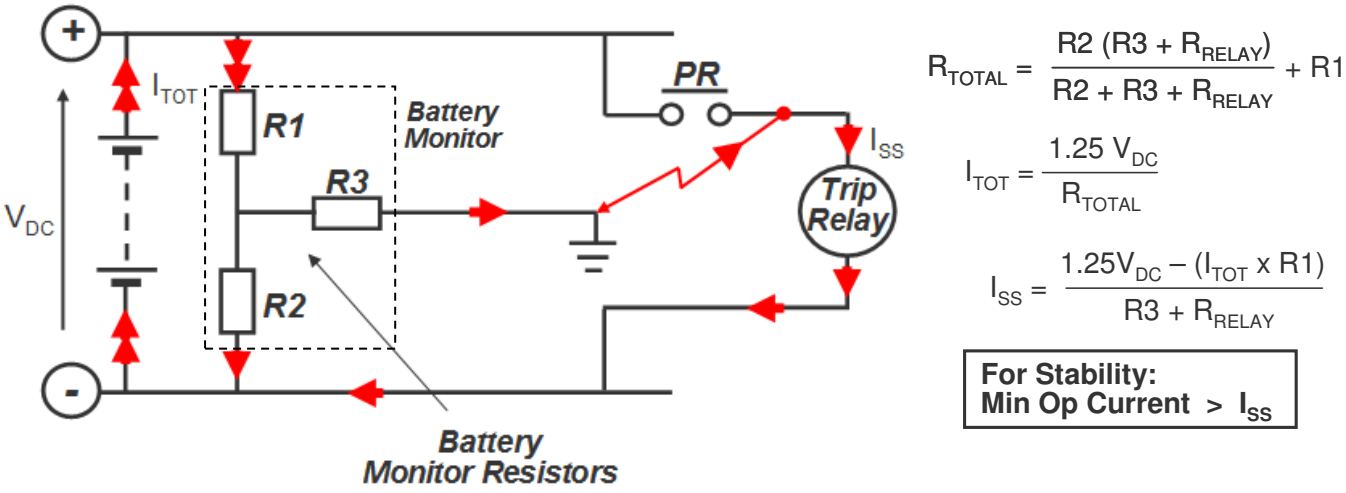


Figure 3.1 – Steady State Relay Current for Centre Tapped Battery

Figure 3.1 clearly shows a positive rail earth fault results in a steady state current through the relay operating coil. It must be ensured that the steady state current (I_{SS}) is less than the relay minimum operating threshold. In most cases, the battery monitor resistances are sufficiently large to prevent mal-operation of the connected relay, which is fortunate as it is often difficult to obtain operating currents for auxiliary relays. Tripping relays, on the other hand, have clearly defined minimum operating currents (see section 2.1.2), which permits their suitability to be confirmed with ease; although it is highly unlikely there will be sufficient current to cause a mal-trip

3.1.2. Opto isolated inputs – steady state voltage

In general, opto inputs have a very large and none linear input impedance, which limits the steady state current to a few milli-amperes at most. Given their low burden design it is sensible to consider optos as voltage operated devices, with infinite input impedance, rather than current operated. For this reason, the voltage presented to the opto must be evaluated to ensure that it is below the opto pick threshold (V_{PU}).

Figure 3.2 illustrates the current path and the equation for calculating the parallel resistor value to ensure steady state stability voltage during the battery earth fault. For simplicity, the equation assumes infinite opto impedance and negligible R3.

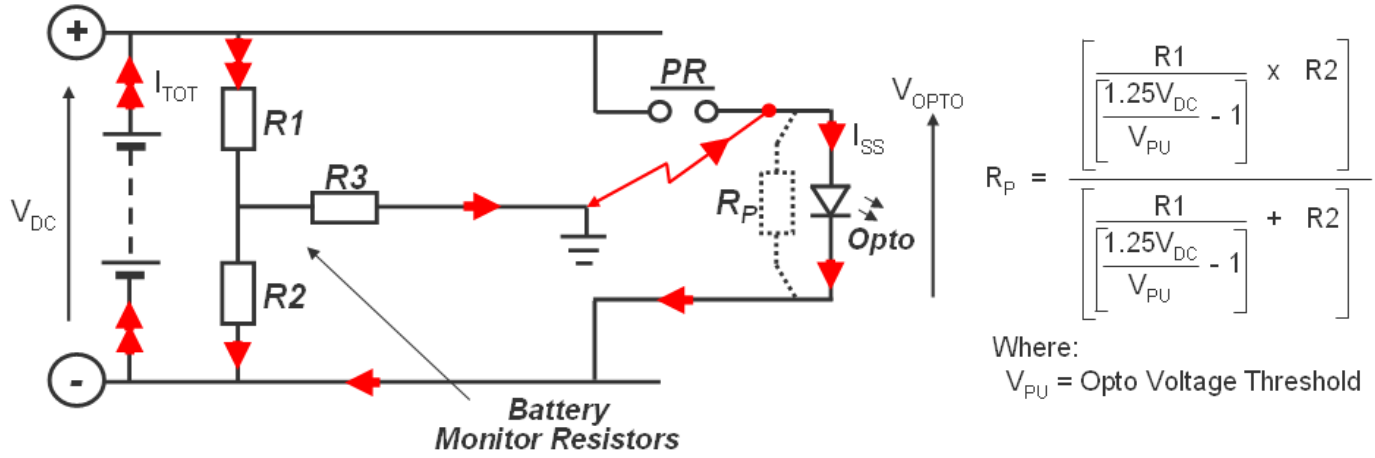


Figure 3.2 – Steady State Opto Voltage for Centre Tapped Battery

Selection of R_P is critical for optos without a selectable opto threshold such as MiCOM Px20 and Px30. Such devices have a typical fixed threshold of only 19 volts (depending upon the model) making them susceptible to the effects of battery earth faults. However, the settable opto threshold in Px40 and Agile relays permits a setting value above the maximum expected voltage of 0.625 V_{DC}, thus providing steady state and transient stability. Transient stability, on centre tapped batteries is discussed in the following section.

NOTE: The value of "0.625", typical for centre tapped battery systems, assumes that R1 and R2 are equal and that the battery is under boost charge conditions (i.e. V_{OPTO} = 0.5 x 1.25 x V_{DC}).

3.2. CENTRE TAPPED BATTERY – TRANSIENT STABILITY (CAPACITANCE DISCHARGE)

Whilst it is relatively simple to assess the steady state stability of a relay or opto circuit, transient stability is more difficult to determine. The transient effects of a battery earth fault are dependent upon the type and length of cable in the DC wiring. Naturally, wiring length will vary from one substation to another, leading to varying degrees of inter-core capacitance. ESI 48-4 EB2 standards stipulate capacitance discharge immunity for tripping relays up to 10µF. While this may seem excessive, relays designed to this standard will almost certainly be suitable to any substation irrespective of its size and wiring length. Low burden relays on the, other hand, are not tested to such standards and will therefore be more susceptible to operation with battery earth faults unless additional measures are taken (see section 3.6).

Much like low burden relays, opto inputs are also susceptible to capacitance discharge from the DC wiring. The pre-fault voltages across the stray wiring capacitances are illustrated figure 3.3. To improve stability, a parallel

resistor (R_P) should be employed to discharge the capacitance before the opto has the opportunity to mal-operate. To discharge the capacitance in sufficient time so as not to cause operation, the R_P value will normally be much smaller than that calculated for steady state stability. Should the calculated R_P value be inappropriate, in terms of current drain and wattage, it may be necessary to consider "double pole switching" as discussed in section 3.6.

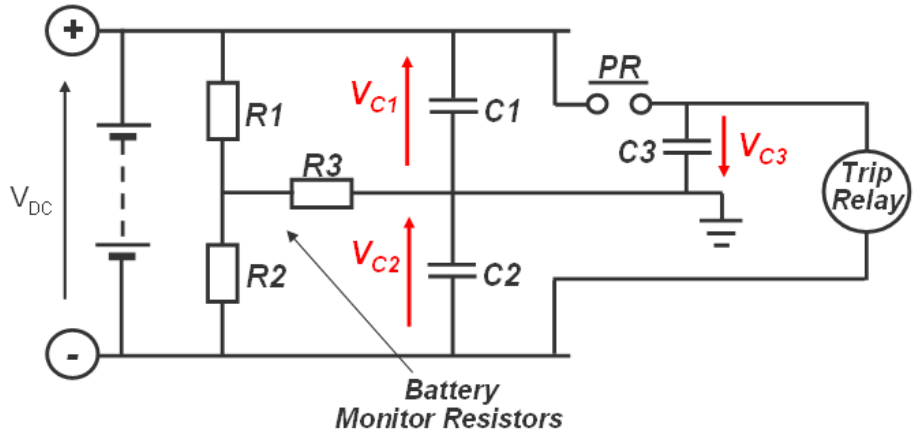


Figure 3.3 – Pre-fault voltages across stray wiring capacitance

3.2.1. Tripping / Auxiliary Relays – capacitance discharge

In order to comply with ESI 48-4 EB2 standards all high burden tripping relays are tested for immunity to capacitance discharge. The test involves discharging a 10µF capacitor initially charged to 1.2 x the upper nominal voltage; which equates to 150V for a 110/125V relay. It is highly unlikely that low burden tripping relays and auxiliary relays will be stable for this condition, hence their use tends to be limited to local wiring runs inside the same panel.

Figure 3.4, illustrates the discharge path and current equation for a positive rail earth fault. C1 and C2 represent the positive and negative rail inter-core capacitances respectively. Ironically, for positive rail faults it is the negative rail capacitance (C2) that drives the discharge current through the relay.

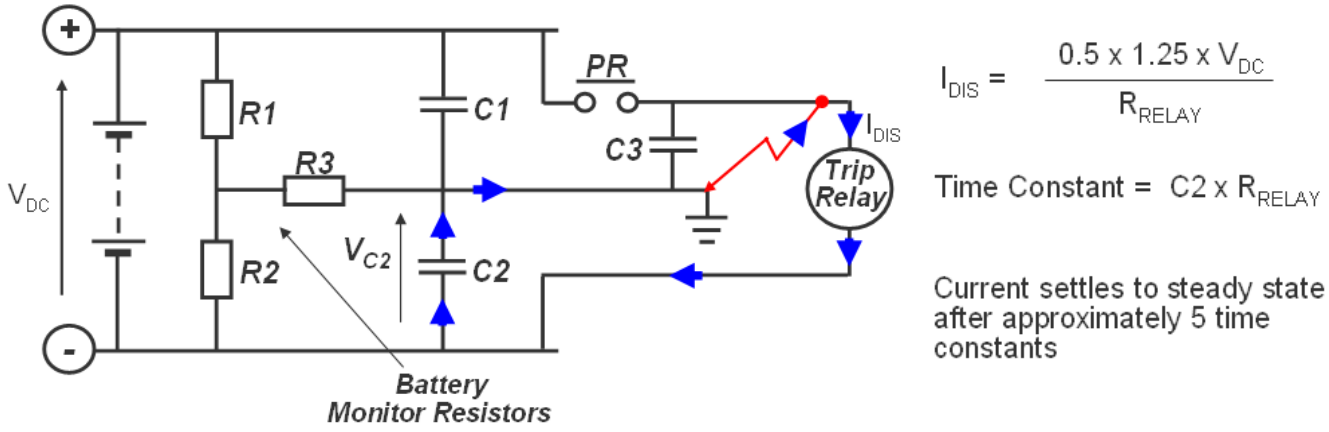


Figure 3.4 – Transient Relay Current for Centre Tapped Battery

To ensure stability, it is essential that the discharge current (I_{DIS}) decays below the relay current threshold before the relay operates. For auxiliary relays the threshold is very low, but the operating time is typically 20ms. Tripping relays, on the other hand, have a higher operating threshold but operate in less than 10ms. The following example demonstrates the need for tripping relays as against auxiliary relays on circuits with long wiring runs where the inter-core capacitance may be large :-

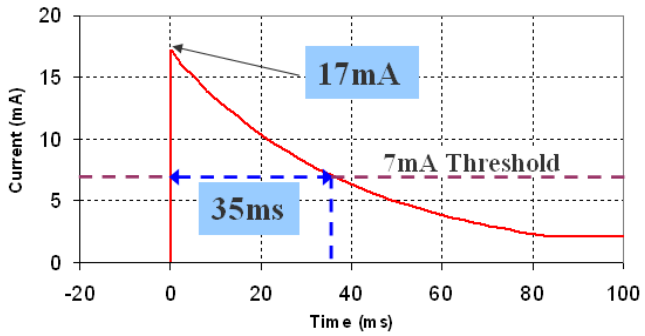
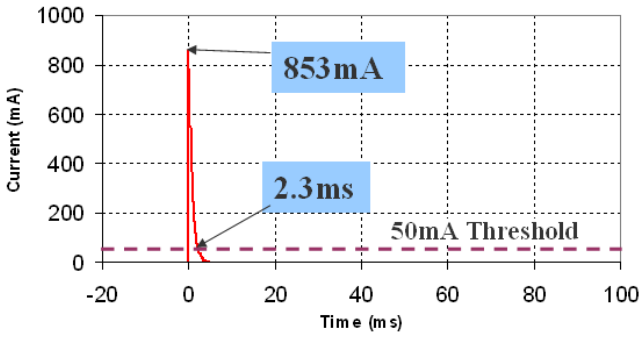
EXAMPLE 1

Compare the performance of an MVAA21 auxiliary relay with an MVAJ21 tripping relay for capacitance discharge. Assume :-

Inter-core capacitance = 10µF (to comply with ESI 48-4 EB2)

Battery voltage = 110V

Fault occurs during boost charging on a centre tapped battery

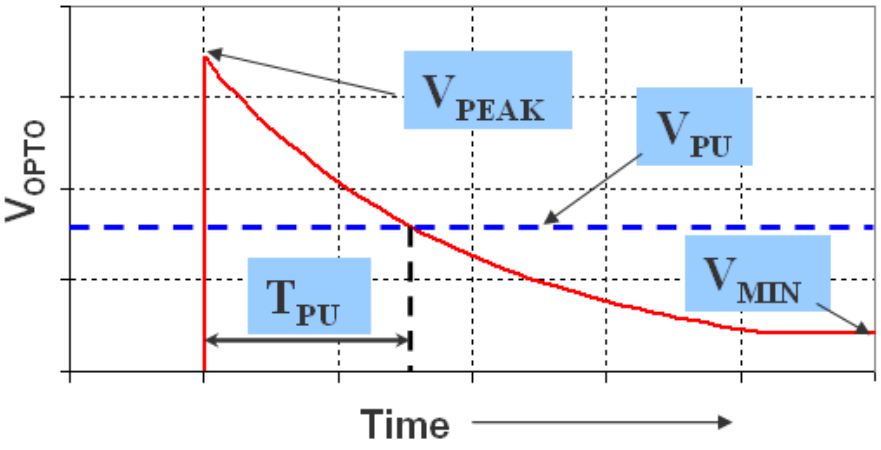
MVAA21 – (Low burden auxiliary relay)	**MVAJ21 – (High burden tripping relay)**
Relay Parameters: Burden = 3W, R_{RELAY} = 4kΩ, Op Current = 7mA	Relay Parameters: Burden = 150W, R_{RELAY} = 81Ω, Op Current ≥ 50mA
Discharge current (I_{DIS}) = $\frac{0.5 \times 1.25 \times 110}{4000}$ = 17mA Time constant = 10×10^{-6} x 4000 = 40.3ms Giving a discharge profile as follows :-  Currents takes longer than 20ms operating time to decay below the 7mA threshold, hence the relay will be unstable. **∴ MVAA21 unsuitable for tripping**	Discharge current (I_{DIS}) = $\frac{0.5 \times 1.25 \times 110}{81}$ = 853mA Time constant = 10×10^{-6} x 81 = 0.81ms Giving a discharge profile as follows :-  Discharge current falls below 50mA threshold in approximately 2.3ms (i.e. much less than 10ms operating time). Pulse duration is insufficient to cause mal-operation **∴ MVAJ21 suitable for tripping**

3.2.2. Opto isolated inputs – capacitance discharge (centre tapped battery)

To ensure transient opto stability for centre tapped batteries a parallel resistor is often, but not always, required. Opto's with fixed thresholds below 0.625 V_{DC} will require a parallel resistor to discharge the capacitor before the

opto recognition time elapses. Consequently, MiCOM Px40 relays, with their adjustable opto threshold, will be stable for a battery earth fault without the need for a parallel resistor.

Another factor that determines stability of the opto is the recognition time (T_{PU}). Opto's with AC filtering tend to employ a 12ms delay (at 50Hz) to provide immunity against induced AC signals. Opto's without this feature, or relays where it has been disabled, will be very susceptible to the discharge caused by an earth fault. In some cases the recognition time may be as low as 200µs. Such cases may require other means such as "double pole switching", discussed later, in order to guarantee stability. Figure 3.5 shows the discharge voltage and the equation for calculating the parallel resistor.



$$V_{OPTO} = V_{MIN} + (V_{PEAK} - V_{MIN}) \cdot e^{\left[\frac{-t}{C2.R_P}\right]}$$

Where:

$$V_{PEAK} = 0.5 \times 1.25V_{DC}$$

$$V_{MIN} = 1.25V_{DC} \times \left[\frac{R2//RP}{R1+(R2//R_P)}\right]$$

Figure 3.5 – Transient Opto Voltage for Centre Tapped Battery

The equation for V_{OPTO} in figure 3.5 clearly shows that both the opto voltage (V_{OPTO}) and the steady state voltage (V_{MIN}) are dependent upon the R_P. Since we now have two unknown quantities in the equation, R_P should be selected either empirically from test data or via iterative methods.

Using an iterative calculation method and assuming a 19V threshold with a 200µs recognition time, the R_P equates to 15.5Ω. Whilst this will provide stability for a transient fault, the continuous burden for normal opto operation will be a ridiculous 9A or 1.2kW. Clearly, for applications where the opto's have a low voltage threshold and a fast recognition time other means should be investigated such as double pole switching.

3.3. CENTRE TAPPED BATTERY – NEGATIVE RAIL FAULTS

Section 3.1 and 3.2 primarily discuss the issue associated with faults on the positive rail of the trip wiring. Naturally, faults can occur on any part of the DC wiring resulting in alternative current paths throughout the circuit. Negative rail faults give rise to capacitive discharge current flowing in the reverse direction through the relay or opto circuit. Devices that are polarity conscious will be unaffected by such faults, however relays or opto's with rectifier circuits will be susceptible to the destabilising effects of negative rail battery earth faults.

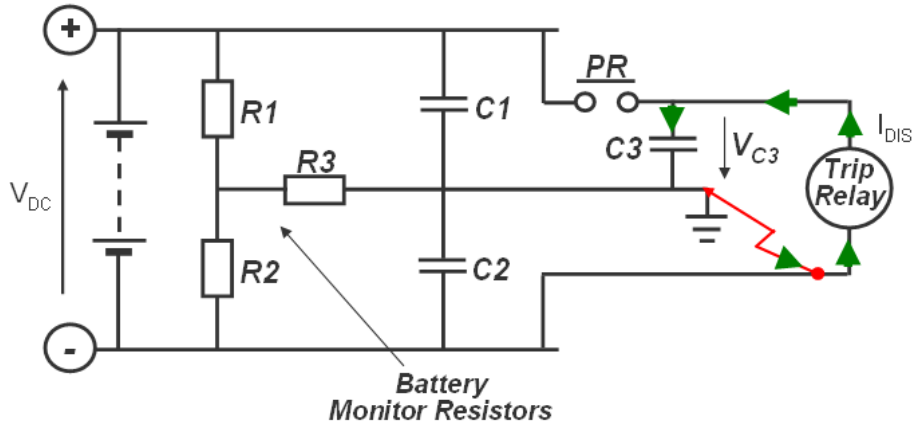


Figure 3.6 – Transient Discharge For Negative Rail Fault

As can be seen in figure 3.6, the transient discharge current passes through the protection device in the reverse direction. In practice the discharge current tends to be smaller than those produced by the positive rail. This is due to the fact that C3 is isolated from the trip supply by the protective relay contact (PR) and that it only holds trapped charge from pervious protection operations. Furthermore, the trapped charge will tend to decay with time as it discharges through the humidity in the asmoshere.

As it is difficult to determine the precise discharge levels, it is sensible to assume that they will be similar in magnitude to those experienced during positive rail faults. Based on this assumption, similar calculations can be performed to check the devices suitability. However, these calculations are only required if the protection device is NOT polarity conscious.

3.4. NEGATIVE EARTHED BATTERIES

Earth faults on negative earthed batteries result in no current flowing through the trip relay / opto input, irrespective of the fault position. Referring to figure 3.7, it can be seen that a fault at position F1 effectively shorts out the relay / opto, whereas a fault at F2 has no impact as the rail is already earthed. Subsequently, for systems with negative earthed batteries, no special action need be taken to ensure relay stability.

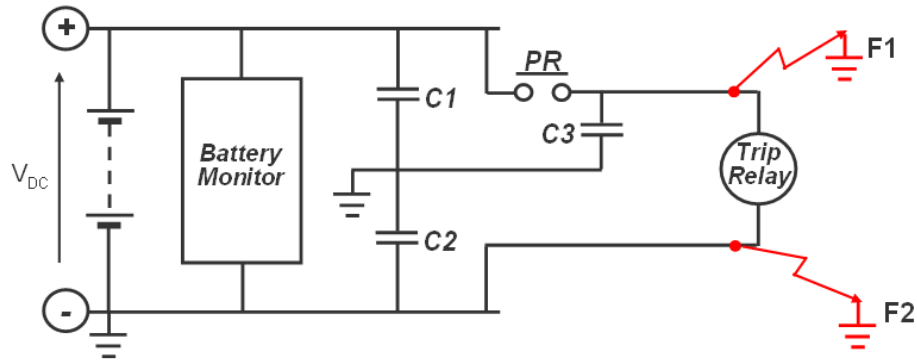


Figure 3.7 – Earth Faults On Negative Earthed Battery

Whilst not shown, faults on the positive earthed batteries also result in zero current through the relay / opto input.

3.5. UNEARTHED BATTERIES

Much like centre tapped batteries, unearthed battery systems can produce a discharge current through the relay / opto circuit during earth faults. However, unlike centre tapped battery systems, unearthed arrangements can give rise to an initial discharge voltage up to nominal voltage (V_{DC}) instead of 0.5 V_{DC}. The actual voltage depends upon the comparative length and wiring type of the positive and negative rails. Figure 3.8 below, illustrates the transient current discharge paths during a positive rail battery earth fault.

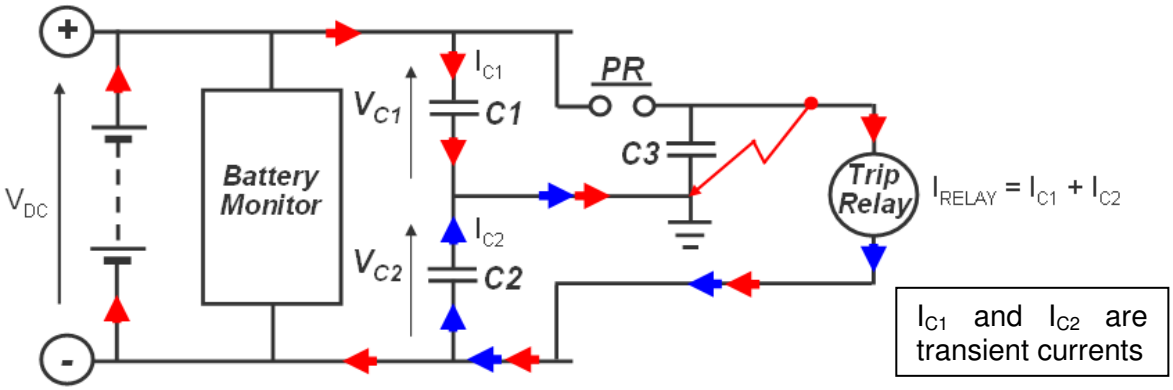


Figure 3.8 – Earth Fault On Unearthed Battery

Referring to figure 3.8 above, the maximum discharge voltage and current occurs when V_{C1} tends to zero and V_{C2} tends to V_{DC}. This coincides with C1 being greater than C2 or, for simplicity, when the positive rail is longer than the negative. During the fault C2 discharges to zero through the relay / opto circuit, whereas C1 charges to V_{DC}.

With such battery systems it is even more important that high burden devices (ideally EB2 compliant) be employed, particularly when the device is required to operate a circuit breaker either directly or indirectly via intertripping. For opto circuits, a parallel resistor may be employed to improve the stability, however the calculation method is somewhat different to that discussed in section 3.2.2 as there is no steady state component to consider.

Transient stability for opto circuits is discussed in the following section.

3.5.1. Opto isolated inputs – capacitance discharge (unearthed battery)

As previously mentioned the transient voltage produced during a battery earth fault on an unearthed battery system can result in a voltage equivalent to V_{DC} across the opto. Unlike centre tapped battery systems however, an opto voltage threshold may be insufficient to give stability thus leading to a need for a parallel resistor R_P. The actual opto voltage can be calculated using the equation shown below :-

$$V_{OPTO} \approx -V_{C2\,(Unfaulted)} \approx -1.25 \times V_{DC} \times \frac{C1}{(C1+C2)}$$ ..... Assuming linear leakage current for C1 & C2

Hence as the ratio of C1 to C2 increases so does V_{OPTO}, up to a maximum of V_{DC}. Therefore, assuming the maximum voltage peaks at V_{DC} and the battery is on boost charge, the parallel stability resistor can be calculated at follows:-

$$R_P = \frac{-T_{PU}}{C \times Ln\left[\frac{V_{PU}}{1.25V_{DC}}\right]}$$

Where: T_{PU} = Opto pick-up delay

C = Largest rail capacitance

V_{PU} = Opto pick-up threshold

V_{DC} = Nominal DC supply voltage

Should the value of R_P be prohibitive in terms of wattage, alternative methods should be considered, such as "double pole switching".

3.6. DOUBLE POLE SWITCHING AND NEGATIVE BIASING RESISTORS

Double pole switching is a technique where by the positive and negative rails are switched instead of just one of them. Essentially the current paths are interrupted on both rails, which prevents any mal-operations due to capacitance discharge. This technique allows low burden devices to be used, such as auxiliary relays and optos, where normally only high burden (EB2) devices would suffice.

In some circumstances a high value resistor, typically 100kΩ, is connected across the contact in the negative rail to minimise corrosion of the battery terminals. This negative biasing resistor, as it sometimes known, limits the capacitance discharge current to typically 0.7mA at 110V, thus preventing any unwanted tripping during earth faults. Figure 3.9, illustrates how the double pole switching is employed together with the optional negative biasing resistor.

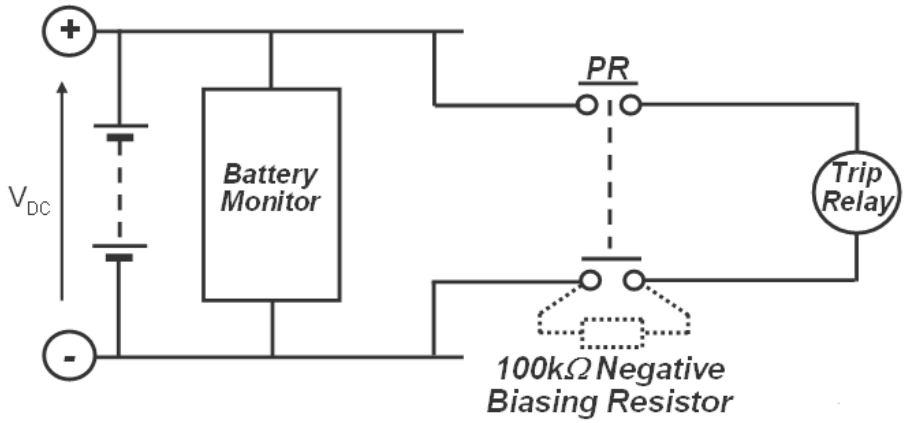


Figure 3.9 – Example of Negative Biasing Resistors

3.7. MICOM AGILE OPTO INPUTS

MiCOM AGILE relays employ a novel type of opto which provides immunity to AC interference and capacitance discharge. The design utilises a switchable shunt impedance, inside the relay, that lowers the opto impedance for approximately 500µs. Lowering the impedance for this period is sufficient to discharge the capacitance before the opto can operate. This technique is superior to the parallel resistor method, as it is unnecessary to apply the AC filtering (12ms delay) in order to achieve discharge immunity. Removing the 12ms delay also allows MiCOM AGILE optos to fully conform to the ESI 48-4 EB2 standard as their operating time will be less than 10ms.

4. AC INTERFERENCE PROBLEMS

All substation wiring is subject to electrical interference of some form. Interference can cause a potential difference between cores and between cores & earth. These voltages are also known as transverse and longitudinal respectively. Longitudinal voltage (cores to earth), which tends to be the largest of the two, is of critical importance when determining insulation requirements for substation wiring, however it is the transverse voltage (between cores) that creates the most interference issues for auxiliary relays and opto inputs. The two main factors that influence the level of transverse voltage are:-

- Inductive coupling
- Capacitive coupling

Inductive coupling is predominantly caused by faults on adjacent current carrying conductors. Capacitive coupling, on the other hand, can be produced by sharing the DC multi-core cable with CT circuits or substation heater supplies. Often ignored is the less severe coupling from VT circuits, which is due to the voltage being typically less than 150V during fault conditions.

The following section discusses the AC immunity issues faced by both hinged armature relays and opto inputs, together with the testing that such devices undergo. This section also offers advice on how to minimise interference issues as well as discussing some of the solutions available in relays in use today.

4.1. INDUCTIVE COUPLING

As previously mentioned, AC interference from inductive coupling is predominantly caused by the fault current in adjacent primary conductors. However, the magnitude of the transverse voltage is dependent upon many factors, most notably the magnitude of the fault current, the conductor spacing and the soil resistivity. With sufficient data an approximate magnitude can be calculated to check the stability of the relay. Where any doubt arises about the relays immunity special measures should be taken, which may include double pole switching (see section 3.6), using screened twisted cable as well as using specialist AC immune relays / optos.

4.1.1. Evaluation of transverse voltage from inductive coupling

The following equations can be used to approximate the transverse voltage in non-twisted cable in close proximity to adjacent current carrying conductors :-

Transverse voltage (Vc) = $\frac{1}{2} j I_F \omega M$

Where:

I_F = Maximum primary fault current
M = Mutual inductance between primary and secondary conductors

However, mutual inductance (M) varies with the conductor material, spacing and soil resistivity. The full equation is shown below :-

$$M = 2\times10^{-4}\, r \times Ln\left[\frac{\sqrt{a^2+\left(b+800\sqrt{2\pi\rho/\omega}\right)^2}}{\sqrt{a^2+b^2}}\right]$$

And

$$r = \left[\frac{1}{\sqrt{1 + (Dd/2\,\Delta^2)^2}} \right] \qquad \Delta \approx 1260 \times \sqrt{\frac{1/\gamma}{\omega\mu}}$$

Where:

- a = Mean distance between primary & secondary
- b = Height of primary conductor
- ρ = Earth resistivity (Ωm^{-1})
- r = Coefficient of screen
- D = Shield external diameter (m)
- d = Thickness of shield (m)
- Δ = Depth of field penetration in to shield (m)
- μ = Permeability of shield material (H/m)
- γ = Conductivity of shield material ($\Omega^{-1}m$)
- ω = Angular frequency = 2πf (radians / sec)

4.1.2. Practical example of inductive coupling

The following example demonstrates the voltages that may be experienced in a typical Grid substation. A 37 core armoured multi-core cable (7/0.67mm) cable has been chosen as it is commonly used for DC substation wiring. Table 4.1 shows the typical mutual inductances for steel and aluminium armoured cable with various levels of earth resistivity.

Earth Resistivity	**Mutual Inductance (mH/km)**	
	Steel Armour μ = 300 H/m γ = 10.2 x 10^6 Ωm	**Aluminium Armour** μ = 1 H/m γ = 35 x 10^6 Ωm
Low = 30 Ωm	0.062	0.88
Medium = 100 Ωm	0.071	0.99
High = 1000 Ωm	0.087	1.22

Table 4.1 – Mutual Inductance for Steel and Aluminium Armoured Cable

Using the figures shown above and assuming a 60kA fault level with a 6.75m separation between primary conductors and the DC wiring, the typical transverse voltages are shown below.

Earth Resistivity	**Induced Voltage (V/m)**	
	Steel Armour	**Aluminium Armour**
Low = 30 Ωm	0.58	8.3
Medium = 100 Ωm	0.67	9.33
High = 1000 Ωm	0.82	11.5

Table 4.2 – Induced Voltage for Steel and Aluminium Armoured Cable

Whilst the figures in table 4.2 imply that the induced voltages are quite large, particularly for aluminium armoured cable, the voltage source will be weak and unable to deliver much current to the relay. It is worth noting that cable connected to the relay / opto is effectively open circuit while the trip contact is open, hence the current will be limited by the inter-core capacitance of the multi-core cable. To mimic the weak source, UK grid standards stipulate the relays are tested with a 100nF capacitor in series with the 250V rms AC voltage source (NGTS 2.13) and the coil / opto as shown in figure 4.1.

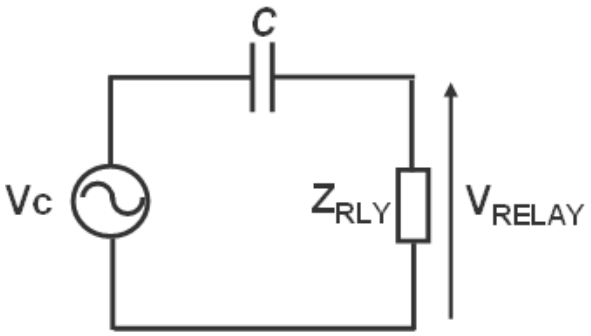


Figure 4.1 – Equivalent Circuit of AC Induced Signals

The following example illustrates the behaviour of auxiliary relays, trip relays and opto inputs for induced AC voltages assuming the equivalent circuit shown in figure 4.1.

EXAMPLE 2

Compare the performance of an MVAA21 auxiliary relay with an MVAJ21 tripping relay and an opto input for induced AC signals. Assuming data from table 4.2 and :-

Inter-core capacitance = 100nF (to comply with ESI 48-4 EB2)

Earth Resistivity = 30Ωm (low)

Aluminium Armoured Cable = 8.3 V/m

Cable length = 50 meters

Therefore:

Induced voltage (Vc) = 8.3 x 50 = 415 Volts

Relay current $= \dfrac{Vc}{\sqrt{R_{RLY}{}^2 + \left(\dfrac{1}{2\pi fC}\right)^2}}$

MVAA21 – (Rectified low burden aux. relay)	**MVAJ21 – (Rectified high burden trip relay)**
Relay Parameters: Burden = 3W, R_{RELAY} = 4kΩ, Op Current = 7mA	Relay Parameters: Burden = 150W, R_{RELAY} = 110Ω, Op Current ≥ 50mA
Relay current = $\dfrac{415}{\sqrt{4000^2 + \left(\dfrac{1}{2\pi \times 50 \times 100 \times 10^{-9}}\right)^2}}$ = <u>12.9mA</u> Current is above the pick-up threshold, hence ***MVAA21 UNSTABLE***	Relay current = $\dfrac{415}{\sqrt{110^2 + \left(\dfrac{1}{2\pi \times 50 \times 100 \times 10^{-9}}\right)^2}}$ = <u>13.0mA</u> Current is below the pick-up threshold, hence ***MVAJ21 is STABLE***
Opto WITHOUT parallel resistor	**Opto WITH parallel resistor**
Opto Parameters: R_{OPTO} = 36 kΩ, Parallel R (Rp) = None Op Voltage = 19V	Opto Parameters: R_{OPTO} = 36 kΩ, Parallel R (Rp) = 1 kΩ, R_{OPTO} // Rp = 973Ω, Op Voltage = 19V
Opto current = $\dfrac{415}{\sqrt{36000^2 + \left(\dfrac{1}{2\pi \times 50 \times 100 \times 10^{-9}}\right)^2}}$ = 8.6mA Opto voltage = 0.0086 x 36000 = <u>310V</u> Voltage is above the pick-up threshold hence the ***opto is UNSTABLE (assuming no AC filtering)***	Total Current = $\dfrac{415}{\sqrt{973^2 + \left(\dfrac{1}{2\pi \times 50 \times 100 \times 10^{-9}}\right)^2}}$ = 13.0mA Opto voltage = 0.013 x 973 = <u>12.68V</u> Voltage is below the pick-up threshold hence ***opto is STABLE***

The example above clearly shows that low burden relays and optos without parallel resistors or AC filtering are susceptible to induced voltages. This issue is of particular importance where signalling of alarms, for devices such

as buchholz, is concerned. Buchholz relays commonly use follower devices to signal alarms or even for tripping purposes. When the AC immunity of a device is in doubt, it is recommended that tripping relays or optos with parallel resistors are used. For situations where the voltage is very high, then optos with AC filtering could be used, at the expense of operating time. Alternatively, a screened twisted cable could be considered.

4.2. CAPACITIVE COUPLING

Capacitive coupling between CT circuits and the DC wiring is only a problem when they share the same multi-core cable. Similar problems can occur when sharing the DC wiring with the 220V substation heater supplies. VT circuits, on the other hand, are not so problematic due to the small VA present in the circuit.

It is widely accepted that high impedance busbar protection schemes are the most onerous of circuits to share the DC wiring with. During internal fault conditions the voltage across the CT secondary circuit can be as high as 3kV. Such a high secondary voltage can give rise to a significant leakage current through the DC relay or opto. Figure 4.2 illustrates the current path through the relay / opto together with the resultant equivalent circuit:-

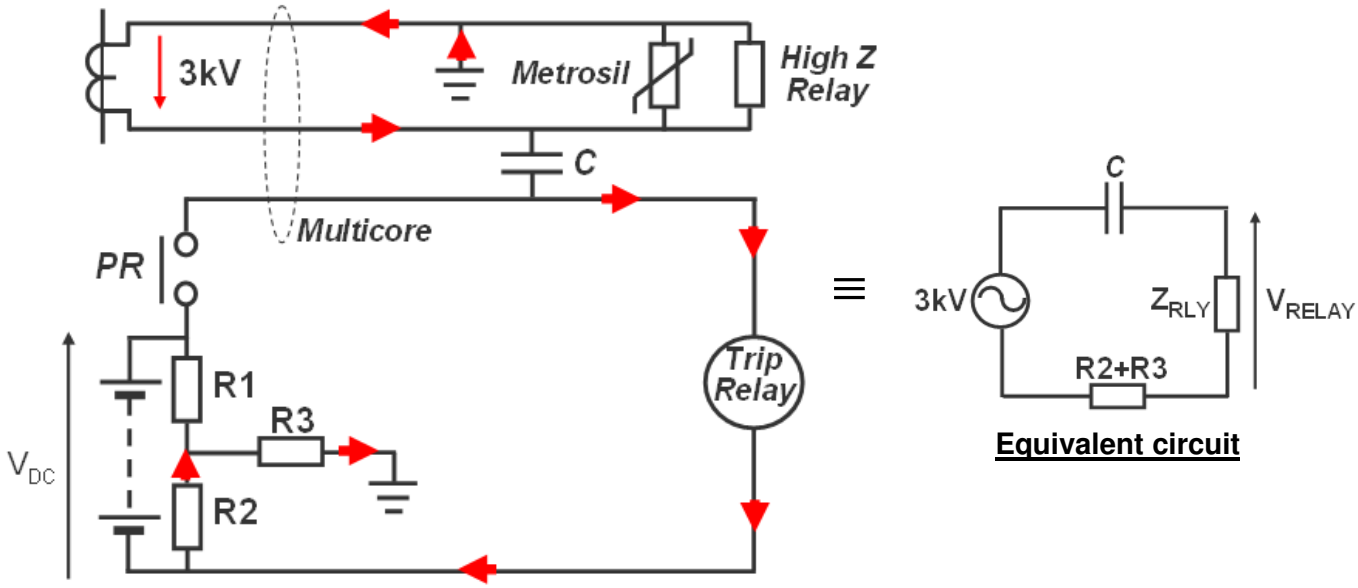


Figure 4.2 – Capacitive coupling from high impedance busbar CT circuit

Figure 4.2 clearly illustrates that the CT and DC circuits are bridged by the capacitance between cores. Inevitably, longer cables will have more capacitance leading to a greater leakage current through the relay, although 100nF is deemed to be the maximum anticipated coupling capacitance. Whilst the battery monitor resistors will also provide additional current limitation, it is feasible that the leakage current may exceed the operating threshold of the relay or opto, particularly if they are of a low burden design. However, it is worth noting that the burden of a tripping relay is quoted for DC applications only and may in fact be a low burden device when AC is applied. This phenomena may cause an unexpected mal-operation particularly when high burden relays have been chosen for their apparent immunity. An example of such an issue is the MVAJ25 relay which has a DC pick threshold greater than 50mA, but an AC threshold of only 4mA. The examples in the following section illustrate how some relays may or may not be stable.

4.2.1. Practical example of capacitive coupling

The following example compares two different tripping relays and also the performance of opto inputs with and without parallel resistors. Coupling is produced by sharing high impedance busbar CT circuits and DC wiring inside a, commonly used, 12 core 7/0.67mm cable with 58nF per km. The maximum wiring length is 500m and the battery is monitored by a BA300 device with R2 and R3 resistance values of 56kΩ and 100Ω respectively.

The following equation is used to calculate the relay / opto voltage and current :-

$$V_{RELAY} = \frac{3kV \times R_{RLY}}{\sqrt{(R_{RLY} + R2 + R3)^2 + (1/\omega C)^2}} \quad \text{and} \quad I_{RELAY} = \frac{V_{RELAY}}{Z_{RLY}}$$

Where C = 0.5 x 58nF = 29nF

MVAA21 – (Rectified low burden aux. relay)	**MVAJ21 – (Rectified high burden trip relay)**
Relay Parameters: Z_{RLY} DC = Z_{RLY} AC = 4kΩ Op Current AC & DC = 7mA,	Relay Parameters: Z_{RLY} DC = Z_{RLY} AC = 110Ω Op Current AC & DC > 50mA
AC Calculation: $V_{RELAY} = \frac{3000 \times 4000}{\sqrt{(4000 + 56000 + 100)^2 + (1/\omega \times 29 \times 10^{-9})^2}}$ = 95.9V $I_{RELAY} = \frac{95.9}{4000}$ = **24mA** Current is below the pick-up threshold, hence ***MVAA21 is UNSTABLE***	AC Calculation: $V_{RELAY} = \frac{3000 \times 110}{\sqrt{(110 + 56000 + 100)^2 + (1/\omega \times 29 \times 10^{-9})^2}}$ = 2.68V $I_{RELAY} = \frac{2.68}{110}$ = **24.3mA** Current is below the pick-up threshold, hence ***MVAJ21 is STABLE***
AC Opto WITHOUT parallel resistor	**AC Opto WITH parallel resistor**
Opto Parameters: R_{OPTO} = 36 kΩ, Parallel R (Rp) = None Op Voltage = 19V	Opto Parameters: R_{OPTO} = 36 kΩ, Parallel R (Rp) = 1 kΩ, R_{OPTO} // Rp = 973Ω, Op Voltage = 19V
AC Calculation: $V_{OPTO} = \frac{3000 \times 36000}{\sqrt{(36000 + 56000 + 100)^2 + (1/\omega \times 29 \times 10^{-9})^2}}$ = **678V** Voltage is above the pick-up threshold hence the ***opto is UNSTABLE***	AC Calculation: $V_{OPTO} = \frac{3000 \times 973}{\sqrt{(973 + 56000 + 100)^2 + (1/\omega \times 29 \times 10^{-9})^2}}$ = **23.6V** Voltage is above the pick-up threshold hence the ***opto is UNSTABLE***

The example above shows that auxiliary relays and even optos with parallel resistors can be unstable when sharing CT wiring with DC circuits. The only stable device was the tripping relay with a rectifier which ensures

that the AC and DC pick-up thresholds are equal. It must be noted, however, that the presence of the rectifier does not guarantee stability for capacitive coupling.

Unlike inductively coupled interference, "twisted pairs" will not provide any immunity as the interference comes from within the same multi-core cable. For this reason alone, it is highly recommended that CT wiring does not share the same multi-core cable as DC circuits. Should this be problematic, or if it means changing vast amounts of substation wiring to correct the problem, then AC immune optos or interposing relays should be used (i.e. type MVAW21).

5. SUMMARY

The following table provides a general guide to illustrate immunity levels for battery earth faults and the two forms of AC interference.

Tripping / Aux Device	Battery Earth Faults			AC Interference		
	Local (Trip relay adjacent to protective relay)	**Remote** (Trip relay remote from protective relay)	**Double Pole Switching**	**Inductive Coupling**	**Capacitive Coupling**	**Double Pole Switching**
Auxiliary Relay	**Generally Stable** Particularly when battery monitors limit the fault current.	**Generally Unstable** Consider using high burden device.	**STABLE**	**Potentially Unstable** Particularly for long cable runs or where aluminium armoured cable is used instead of steal.	**Potentially Unstable** DC wiring should not share the same multi-core as CT wiring.	**Improved Stability** Improves stability if switching is local to auxiliary relay. Provides total capacitive coupling immunity irrespective of switching location.
Low Burden Trip Relay (ESI 48-4 EB1)	**STABLE**	**Generally Unstable** Not recommended for tripping purposes in this case.	**STABLE**	**Potentially Unstable** More stable than auxiliary relay, but not ideal. Recommend twisted pairs.	**Potentially Unstable** DC wiring should not share the same multi-core as CT wiring.	**Improved Stability** As above
High Burden Trip Relay (ESI 48-4 EB2)	**STABLE**	**STABLE**	**STABLE**	**Generally Stable** Except for extreme circumstances. Where problems arise twisted pairs are recommended or use interposing relay.	**Generally Stable** Except for extreme circumstances. Ideally DC wiring should not share the same multi-core as CT wiring.	**Improved Stability** As above.
Plain Opto (Fixed 19V Threshold)	**UNSTABLE**	**UNSTABLE**	**STABLE**	**Generally Unstable** Recommend twisted pairs.	**Generally Unstable**. DC wiring should not share the same multi-core as CT wiring.	**Improved Stability** As above.
Opto with Parallel Resistor (Fixed 19V Threshold) (No AC Filtering)	**Generally Stable**	**Potentially Unstable** Parallel resistor may be prohibitively high wattage to be practical.	**STABLE**	**Generally Stable** With appropriate resistor.	**Potentially Unstable**. DC wiring should not share the same multi-core as CT wiring.	**Improved Stability** As above.
Advanced Opto (Px40) (Optional Parallel Resistor) (Variable Threshold) (Optional AC Filtering)	**STABLE**	**STABLE** Parallel resistor and small time delay will be required for unearthed batteries.	**STABLE**	**STABLE** With AC Filtering	**STABLE** With AC Filtering	**STABLE** Not required with AC Filtering activated
Advanced AGILE Opto	**STABLE**	**STABLE**	**STABLE**	**STABLE**	**STABLE**	**STABLE** Not required with AC Filtering

				With AC Filtering	With AC Filtering	activated

REVIEW HISTORY

Issue	Name	Position
A	A Wixon	Senior Applications Engineer

VERSION CONTROL

Issue	Author(s)	Reason for change	Date
A	A. Wixon	Original.	09/02/12